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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,938	12/12/2003	Lee W. Atkinson	200300687-1	1470

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EXAMINER	
PHAM, THOMAS K	

ART UNIT	PAPER NUMBER
2121	

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,938	ATKINSON ET AL.	
	Examiner	Art Unit	
	Thomas K. Pham	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. This is in response to the request for re-consideration filed 9/28/2006.

2. Applicants' arguments have been fully considered but they are not persuasive.

Quotations of U.S. Code Title 35

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim Rejections - 35 USC § 102

7. Claims 1, 5, 6, 12, 14-16, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,967,522 ("Chandrakasan").

Regarding claim 1

Chandrakasan teaches the invention including a system, comprising: power management logic is taught as the controllers 20, 70 or 90 of FIG. 2, FIG. 3 and FIG. 5; an electrical load coupled to the power management logic and configurable to operate in accordance with any of a plurality of power states is taught as the controller 20 is coupled to microprocessor 30 (device) to operate accordance to different power states of the microprocessor 30 (see FIG. 2 and Col. 7 lines 36-50); wherein, if an operating voltage for the system is between two thresholds, the power management logic forces the electrical load to operate in a reduced power state is taught as a threshold voltage is selected in combination with a select supply voltage can be utilized to control and reduce the power consumption of a device (see Col. 2 lines 43-52, Col. 5 lines 1-3, Col. 6 lines 18-28 and Col. 14 lines 14-22).

Regarding claim 12

Chandrakasan teaches the invention including a system, comprising: an electrical load configurable to operate in accordance with any of a plurality of power states is taught as the controller 20 is coupled to microprocessor 30 (device) to operate accordance to different power states of the microprocessor 30 (see FIG. 2 and Col. 7 lines 36-50); and power management means coupled to the load for forcing the system to operate in a reduced power state when an operating voltage is between two voltage levels is taught as a threshold voltage is selected in combination with a select supply voltage can be utilized to control and reduce the power

consumption of a device (see Col. 2 lines 43-52, Col. 5 lines 1-3, Col. 6 lines 18-28 and Col. 14 lines 14-22).

Regarding claim 16

Chandrakasan teaches the invention including a power management logic unit configured to operate in a system, comprising: control logic that receives first and second signals (see Col. 7 lines 40-55), determines whether an operating voltage is between first and second reference voltages based on the first and second signals and, if so, causes the system to operate in a non-programmable, reduced performance mode is taught as a threshold voltage is selected in combination with a select supply voltage can be utilized to control and reduce the power consumption of a device (see Col. 2 lines 43-52, Col. 5 lines 1-3, Col. 6 lines 18-28 and Col. 14 lines 14-22).

Regarding claim 18

Chandrakasan teaches the invention including a method, comprising: comparing an operating voltage to a first reference voltage and to a second reference voltage (see Col. 7 lines 40-55); and when the operating voltage is between the two reference voltages, requiring a system to operate in a less than full performance mode is taught as a threshold voltage is selected in combination with a select supply voltage can be utilized to control and reduce the power consumption of a device (see Col. 2 lines 43-52, Col. 5 lines 1-3, Col. 6 lines 18-28 and Col. 14 lines 14-22).

Regarding claim 5

Chandrakasan teaches wherein the system comprises a computer (see Col. 5 lines 1-10).

Regarding claim 6

Chandrakasan teaches the electrical load comprises a CPU coupled to the power management logic and the reduced power state comprises a reduced average clock frequency of a CPU clock (see FIG. 2 and Col. 8 lines 8-12).

Regarding claim 14

Chandrakasan teaches the means for forcing the system to operate in the reduced power state comprises means for reducing a clock frequency associated with a CPU in the system (see Col. 9 lines 16-27).

Regarding claim 15

Chandrakasan teaches means for determining whether the operating voltage is between the two voltage levels (see Col. 14 lines 14-30).

Claim Rejections - 35 USC § 103

8. Claims 2-4, 9-11, 13, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chandrakasan in view of U.S. Patent No. 6,690,652 ("Sadri").

Regarding claim 2

Chandrakasan does not specifically teach a pair of comparators coupling the operating voltage to inputs of the power management logic, each comparator having a reference voltage different from each other.

However, Sadri teaches a power control system with a pair of comparators for comparing operating voltage to the upper threshold and the lower threshold (see Col. 4 lines 39-43) for the purpose of minimizing device power consumption by optimizing power usage in the device (see Col. 4 lines 45-48).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the pair of comparators of Sadri with the power management system of Chandrakasan because it would provide for the purpose of minimizing device power consumption by optimizing power usage in the device.

Regarding claim 3

Chandrakasan discloses an example of a 0.4 V supply voltage and a 0.24 V threshold voltage (see Col. 15 lines 54-67).

It should be noted that the threshold values set forth (e.g. 15.5 VDC and 14.5 VDC) is given very little patentable weight. In the absence of any new or unexpected results, the threshold values are considered to be set to any values operate on a specific device.

Regarding claim 4

Chandrakasan teaches the power management logic determines whether the operating voltage is between the reference voltages (see Col. 6 lines 29-37).

Regarding claim 9

Chandrakasan does not teach if the power management logic determines the operating voltage is above both of the two thresholds, the power management logic permits the system to operate in any one of a plurality of power states.

However, Sadri teaches if the power management logic determines the operating voltage is above both of the two thresholds, the power management logic permits the system to operate in any one of a plurality of power states (see Col. 4 lines 35-37) for the purpose of minimizing device power consumption by optimizing power usage in the device (see Col. 4 lines 45-48).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the power management logic of Sadri with the power management system of Chandrakasan because it would provide for the purpose of minimizing device power consumption by optimizing power usage in the device.

Regarding claim 10

Chandrakasan teaches the power states are programmable (see Col. 8 lines 35-44).

Regarding claim 11

Chandrakasan does not teach if the power management logic determines the operating voltage is below both of the two thresholds, the power management logic causes the system to operate in any one of a plurality of power states.

However, Sadri teaches if the power management logic determines the operating voltage is below both of the two thresholds, the power management logic permits the system to operate in any one of a plurality of power states (see Col. 4 lines 33-35) for the purpose of minimizing device power consumption by optimizing power usage in the device (see Col. 4 lines 45-48).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the power management logic of Sadri with the power management system of Chandrakasan because it would provide for the purpose of minimizing device power consumption by optimizing power usage in the device.

Regarding claim 13

Chandrakasan does not teach means for permitting the system to operate in any of a plurality of power states when the operating voltage is not between the two voltage levels.

However, Sadri teaches permitting the system to operate in any of a plurality of power states when the operating voltage is not between the two voltage levels (see Col. 4 lines 33-37) for the purpose of minimizing device power consumption by optimizing power usage in the device (see Col. 4 lines 45-48).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the power management logic of Sadri with the power management system of Chandrakasan because it would provide for the purpose of minimizing device power consumption by optimizing power usage in the device.

Regarding claim 17

Chandrakasan does not teach the control logic determines whether the operating voltage is not between the first and second reference voltages and, if so, permits the system to operate in a mode that requires more power than the reduced performance mode.

However, Sadri teaches the control logic determines whether the operating voltage is not between the first and second reference voltages and, if so, permits the system to operate in a mode that requires more power than the reduced performance mode (see Col. 4 lines 35-37) for the purpose of minimizing device power consumption by optimizing power usage in the device (see Col. 4 lines 45-48).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the power management logic of Sadri with the power management system of Chandrakasan because it would provide for the purpose of minimizing device power consumption by optimizing power usage in the device.

Regarding claim 20

Chandrakasan teaches the reference voltages comprise a first reference voltage and a second reference voltage and the first reference voltage is higher than the second reference voltage. Chandrakasan does not teach permitting the system to operate in any one of a plurality of programmable modes only if the operating voltage is above the first reference voltage or below the second reference voltage.

However, Sadri teaches permitting the system to operate in any one of a plurality of programmable modes only if the operating voltage is above the first reference voltage or below the second reference voltage (see Col. 4 lines 33-37) for the purpose of minimizing device power consumption by optimizing power usage in the device (see Col. 4 lines 45-48).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the power management logic of Sadri with the power management system of Chandrakasan because it would provide for the purpose of minimizing device power consumption by optimizing power usage in the device.

9. Claims 7, 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chandrakasan in view of U.S. Patent No. 5,991,883 ("Atkinson").

Regarding claim 7

Chandrakasan does not teach the electrical load comprises a display and the reduced power state comprises a dimmed display.

However, Atkinson teaches a system for power conservation in a portable computer system including a dimmed LCD display (see Col. 2 lines 55-63) for the purpose of reducing the power of the display when high performance is not required (see Col. 2 lines 64-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the display system of Atkinson with the system of Chandrakasan for the purpose of reducing the power of the display when high performance is not required.

Regarding claim 8

Chandrakasan does not specifically teach if the power management logic determines the operating voltage is above both of the two thresholds, the power management logic permits the system to operate in a full performance power state.

However, Arkison teaches a video controller set the core voltage to operate in full performance power state when the operating voltage is above certain voltage levels (see Col. 10 lines 17-26) for the purpose of reducing the power of the display when high performance is not required (see Col. 2 lines 64-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the display system of Atkinson with the system of Chandrakasan for the purpose of reducing the power of a device when high performance is not required.

Regarding claim 19

Chandrakasan teaches the reference voltages comprise a first reference voltage and a second reference voltage and the first reference voltage is higher than the second reference voltage. Chandrakasan does not teach permitting the system to operate in a full performance mode when operating voltage is above the first reference voltage or below the second reference voltage.

However, Arkison teaches a video controller set the core voltage to operate in full performance power state when the operating voltage is above certain voltage levels (see Col. 10

lines 17-26) for the purpose of reducing the power of the display when high performance is not required (see Col. 2 lines 64-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the display system of Atkinson with the system of Chandrakasan for the purpose of reducing the power of a device when high performance is not required.

Response to Arguments

In the remarks, the applicants argue that cited reference fails to teach:

I) "if an operating voltage for the system is between two thresholds, the power management logic forces the electrical load to operate in a reduced power state." as to claim 1, 12, 16 and 18.

In response to applicants' arguments,

I) Prior art Chandrakasan (U.S. Patent No. 6,967,522) discloses a controller (power management logic) selects and set a threshold voltage during operation and thus control a power dissipation, wherein the power dissipation is reduced based on the workload requirement, through dynamic adjustment of the supply voltage or the threshold voltage as described below in column 6 lines 18-55.

> Power dissipation may be reduced, for example, when processing rate requirements vary, i.e., workload demand varies, through dynamic adjustment of supply voltage (Vdd) and body bias voltage (Vbb). Forward body bias may be used to increase the dynamic range of device threshold. Forward biasing, however, may degrade performance because diode and parasitic-bipolar emitter currents in a substrate may dominate. Hence, an optimum power point may correspond to a forward body bias at which the operating speed can no longer be improved with increased forward bias.
>
> In a closed control loop, the supply voltage or the threshold voltage may be determined during operation by varying a supply voltage or a threshold voltage, while observing the

power consumption of the device. The observations may be performed on a monitor circuit, rather than on the device itself. In the former case, the supply voltage and/or threshold voltage may be determined prior to device operation by observations on the device, a prototype device or model circuit, for example. The predetermined values may then be stored for use by the device during operation. The predetermined values may be stored, for example, in a lookup table. A lookup table may be implemented via hardware and/or software components that provide permanent or temporary data storage.

Various embodiments implement a dual control loop to cooperatively select and apply a supply voltage and select and set a threshold voltage, and thus control a power dissipation. The following will describe several detailed embodiments that implement control loops for a CMOS device. These embodiments may be categorized as belonging to one of three control loop implementations: dual open loop; dual closed loop; and hybrid loop. These implementations may permit decoupling of supply voltage control and threshold voltage control, for more stable control of power consumption. A device may include voltage controllers, or voltage controllers may be located separately from the device.

It is clear that the invention of Chandrakasan has all the possible combinations of power management for a device including either individual control loop or dual control loop. In both cases, the power dissipation may be reduce (or increase) in conjunction with a predetermined threshold voltage set during operation and according to various operating conditions of the device. Thus, Chandrakasan teaches the limitation set forth in the claims.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner *Thomas Pham*; whose telephone number is (571) 272-3689, Monday to Friday from 7:30 AM - 4:00 PM EST or contact Supervisor *Mr. Anthony Knight* at (571) 272-3687.

Thomas Pham
Patent Examiner

November 27, 2006